A SAR-Assisted Two Stage Pipeline ADC

Article Review

Pietro Pennestrì
p.pennestri@student.utwente.nl

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1 Introduction

1.1 Relevant Specifications & Novelties

The main concept behind this paper is that in a pipeline ADC one extra bit in the first stage improves the linearity of the converter by a factor of $\sqrt{2}$. This behavior is justified by the following relationship[1]

$$\mathrm{DNL} \propto \frac{2^{N-0.5M}}{\sqrt{C_{total}}} \tag{1}$$

reported in [10] and valid when the capacitor mismatches are due to random variations in the interpoly oxide thickness.
Other advantages of a high resolution first stage are:

- 👍 the number of total stages is reduced;
- 👍 requirements on noise and component matching are relaxed.

However, in a standard pipeline architecture, with a high resolution first stage, the following disadvantages are recognized:

- 👎 the THA amplifier has to drive a larger converter;
- 👎 the residue amplifier of the first stage needs a larger gain bandwidth product;
- 👎 the high number of comparators leads to high power consumption.

To overcome these shortcomings, the Authors implemented for the first time in the literature a *SAR assisted* two stages pipeline ADC. The details of the proposed architecture are explained in the following. The main features of the proposed amplifier are summarized in Figure 1.

[1] The nomenclature is the same adopted in the paper.

	65nm Design	90nm Design
SNDR (2MHz input)	66dB (10.7b ENOB)	65.6dB (10.6b ENOB)
Conversion Rate (Fs)	50MS/s	50MS/s
Linearity (12b level)	|INL|<1.5LSB |DNL|<0.75LSB	|INL|<1.6LSB |DNL|<0.8LSB
SFDR (4MHz at -0.5dB FS)	78dB	77dB
Input Range	$2V_{pk-pk}$ differential	$2V_{pk-pk}$ differential
Input Capacitance	1pF differential	1pF differential
Power Supply	1.3V	1.3V
Power Consumption	3.5mW	3.6mW
FOM [P/(Fs*2^{ENOB})]	52fJ/conversion-step	53fJ/conversion-step
Core Area	$0.16mm^2$	$0.16mm^2$
Process	1P9M 65nm CMOS	1P7M 90nm CMOS

Figure 1: Specifications of the proposed ADC

1.2 Application area of the ADC

According to the listed specs, the ADC as shown in Figure 2 is suitable for low power application in the domain of video, cell phones, short range wireless and home internet.

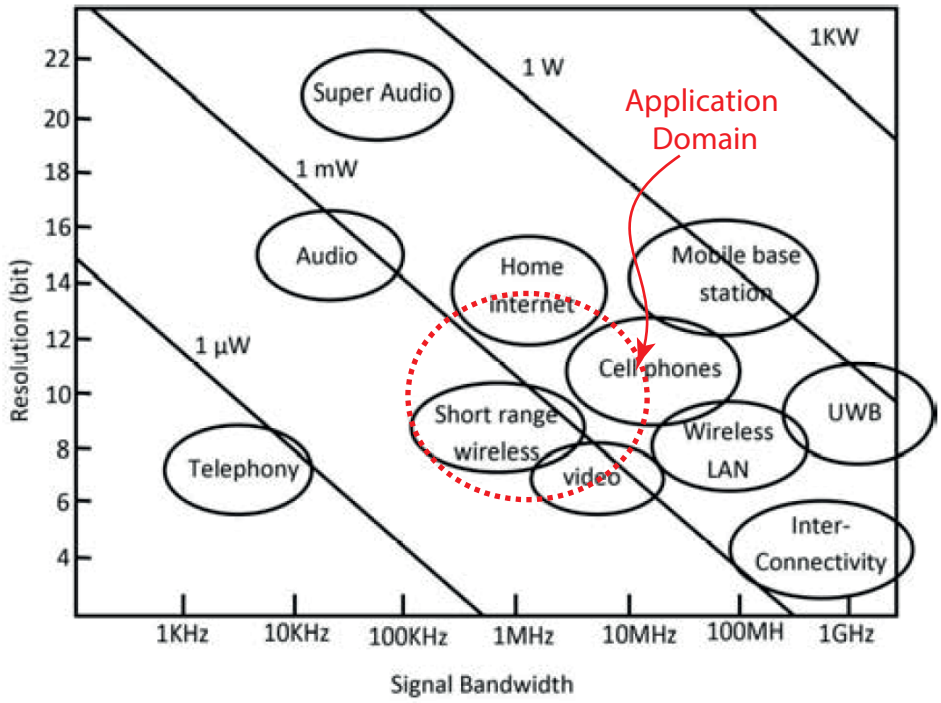


Figure 2: Application Domain. Figure adapted from [7].

2 Architecture of the ADC

The architecture proposed by the Authors is depicted in Figure 3

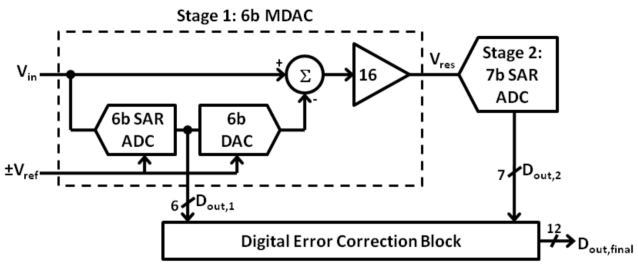


Figure 3: SAR assisted 2 stage pipeline ADC

The architecture is an hybrid between a SAR and a pipeline ADC. In particular the structure is a two stage pipeline ADC. The first stage sub-ADC has a resolution of 6 bit (1 bit of redundancy) and it is implemented with a SAR architecture. The second stage is also implemented with a SAR converter and it has a resolution of 7 bit. The replacement of flash converter with SAR leads to the following considerations:

- 👍 The use of SAR architecture for the first stage reduces the number of comparators from 63 to 1. This implies a reduction both in area and power requirements.
- 👍 In the first stage, the SAR sub-ADC and the MDAC share the same sampling path. Thus, there is no need of calibration techniques trying to compensate for sampling errors.
- 👍 No need of a dedicated front end S/H.
- 👎 SAR architectures are slower then flash ones. This implies a longer decision time for the first stage SAR sub-ADC. Thus, the sample or the hold time for the MDAC is reduced.

Finally, as long as it is available a topology that allows both high resolution and shares the same sampling path, similar performances could be achieved. In the following we will discuss in detail the two stages that compose the ADC.

2.1 First Stage

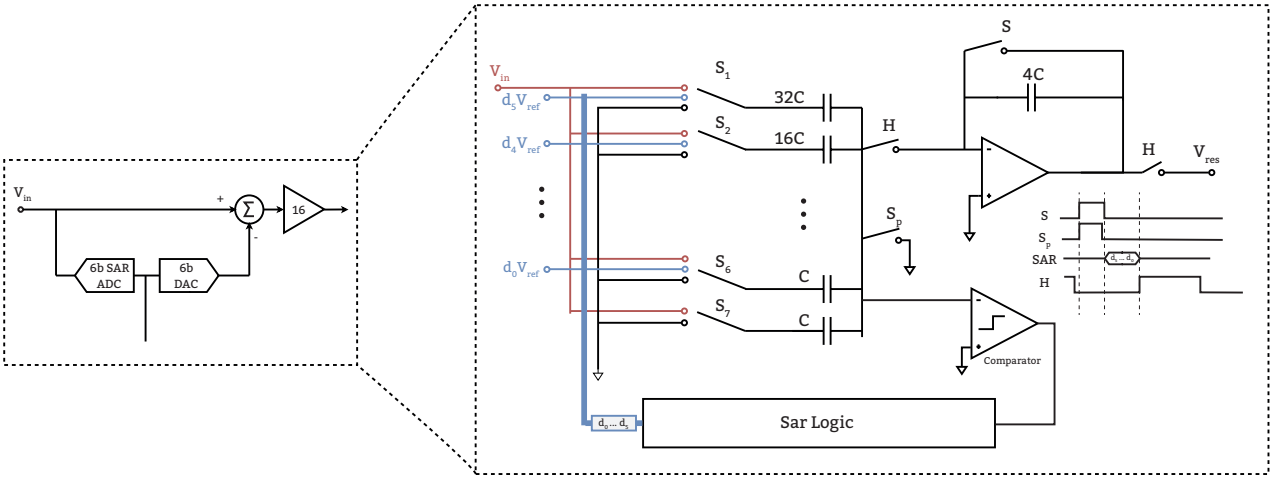


Figure 4: First Stage of the ADC

2.1.1 Analysis

The first stage of the ADC, has 3 phases of operation:

- **Sample Phase**: During this phase switches $[\mathrm{S}_1 ... \mathrm{S}_7]$ are connected to v_{in}. The equivalent circuit is shown in Figure 5 and the total charge stored in capacitors is:

$$Q_{tot} = -64CV_{in} \tag{2}$$

  The amplifier, thanks to the switch H, is isolated from the main circuit to avoid at its input large voltage variation that may occur during the SAR decision phase.

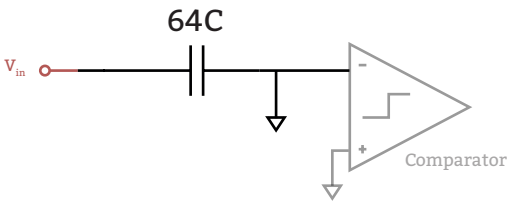


Figure 5: Equivalent circuit during the sample phase

- **SAR phase**. This phase of can be divided into different steps.
  - *Step 1*: Switches S, S_P are opened and $[\mathrm{S}_1 ... \mathrm{S}_7]$ are connected to GND. From charge conservation $V_x = -V_{in}$. The equivalent circuit is shown in Figure 6.

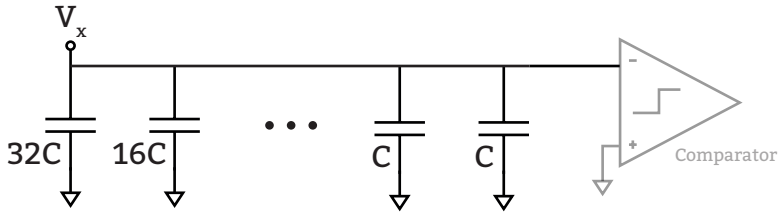


Figure 6: Equivalent circuit during the SAR, step 1 phase

- *Step 2, the determination of the MSB*: Switch S_1 is set into $d_5 V_{ref}$ position. The SAR logic sets d_5 to 1. Switches $[S_2 \dots S_7]$ are kept at ground position. The equivalent circuit is shown in Figure 7

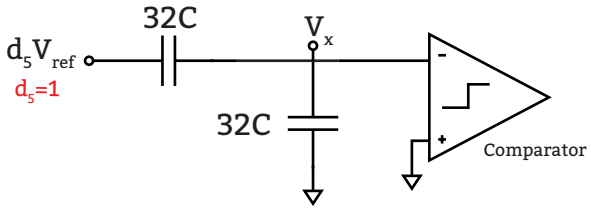


Figure 7: Equivalent circuit during the MSB determination

From charge conservation:

$$-V_{in}2^6C = (V_x - V_{ref})2^{6-1}C + V_x 2^{6-1}C$$
$$V_x = -V_{in} + \frac{V_{ref}}{2} \tag{3}$$

The comparator decides whenever $V_x > 0$. In this case the SAR logic leaves $d_5 = 1$, otherwise it will be set to 0.

- *Step 3, the determination of the MSB - 1:* d_4 bit is set to 1 and all other switches are not modified. The equivalent circuit is shown in Figure 8.

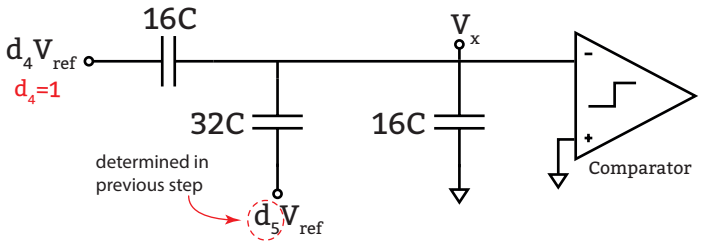


Figure 8: Equivalent circuit during the MSB-1 determination

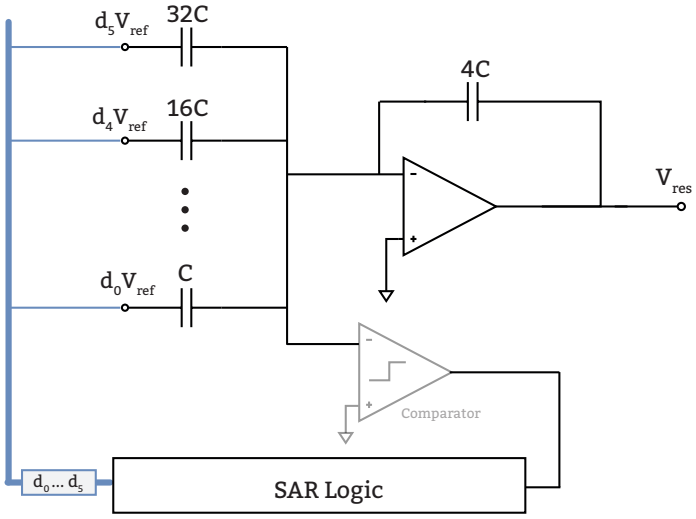
From charge conservation:

$$-64V_{in}C = (V_x - V_{ref})16C + (V_x - d_5 V_{ref})32C + V_x 16C$$
$$V_x = -V_{in} + \frac{V_{ref}}{4} + d_5\frac{V_{ref}}{2} \tag{4}$$

If $V_x > 0$, then the value of d_4 is not modified, otherwise it is set to 0.

The process illustrated in *Step 3* is repeated to determine the remaining bits.

- **Hold Phase** During this phase switches H are closed. The equivalent circuit is shown in Figure 9.



From charge conservation the following expression for V_{res} is deduced:

$$-2^6 C V_{in} = -\sum_{i=0}^{5} d_i V_{ref} 2^i C - V_{res} 4C$$

$$V_{res} = 16\left(V_{in} - \sum_{i=0}^{5} d_i \frac{V_{ref}}{2^6} 2^i\right)$$

Figure 9: Equivalent Circuit during the hold phase

From equation (5), the closed loop gain of the residue amplifier is 16, half of the standard implementation. Moreover, the reduced gain of the amplifier leads to:

- The closed loop bandwidth of the amplifier is increased by two.
- The specifications on the output swing of the amplifier are relaxed.
- Since the signal has **half of the full scale range**, the thermal noise budget in second stage is reduced.

2.2 Second Stage

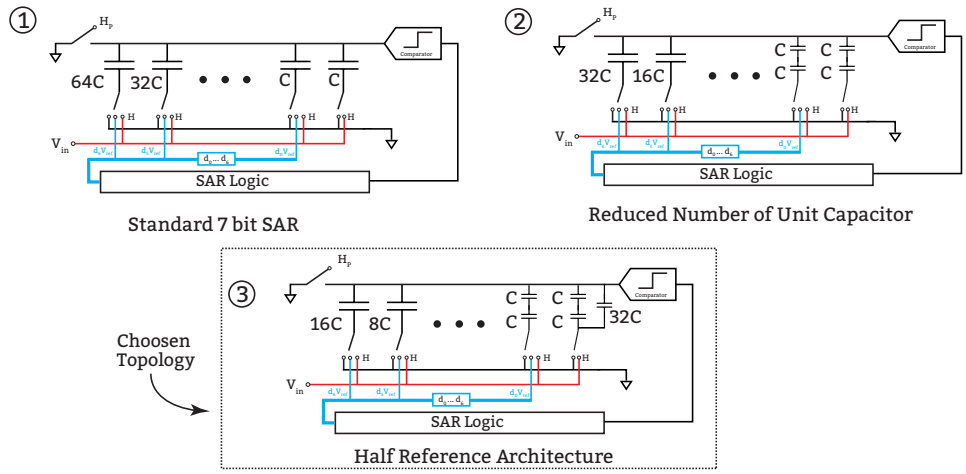


Figure 10: Second Stage Topology

The topology of the second stage is depicted in Figure 10. Since the half gain implementation of the first stage, a standard implementation of a SAR converter is not convenient due to an additional reference voltage of $\pm\frac{V_{ref}}{2}$ requirement. The process to overcome the extra reference voltage is illustrated in Figure 10 and it is explained in the following:

- From the standard architecture the number of unit capacitor is reduced by dividing the value of every capacitance by two. The number of unit capacitance is reduced from 128 to 67. However, this change does not solve the voltage reference problem and raises the $\frac{kT}{C}$ noise.
- The previous structure is modified in such a way that every capacitor is split into two equal parts. The signal is sampled onto the entire capacitor array, but during the decision phase **only one half** of each capacitor is connected to V_{ref}. From now on we will refer to this structure as the *Half Reference* SAR.

From the Figure presented in the article we observe that 1 bit is missing and the order of the bits should be reversed. These issues are illustrated in Figure 11. In Section V of the reviewed article, the Authors claim that in 65 nm architecture the second stage is **not implemented** with the half reference topology. However, from the

information provided, it is not clear if in the 65 nm architecture an additional reference voltage is introduced or the gain of the first stage amplifier is doubled.

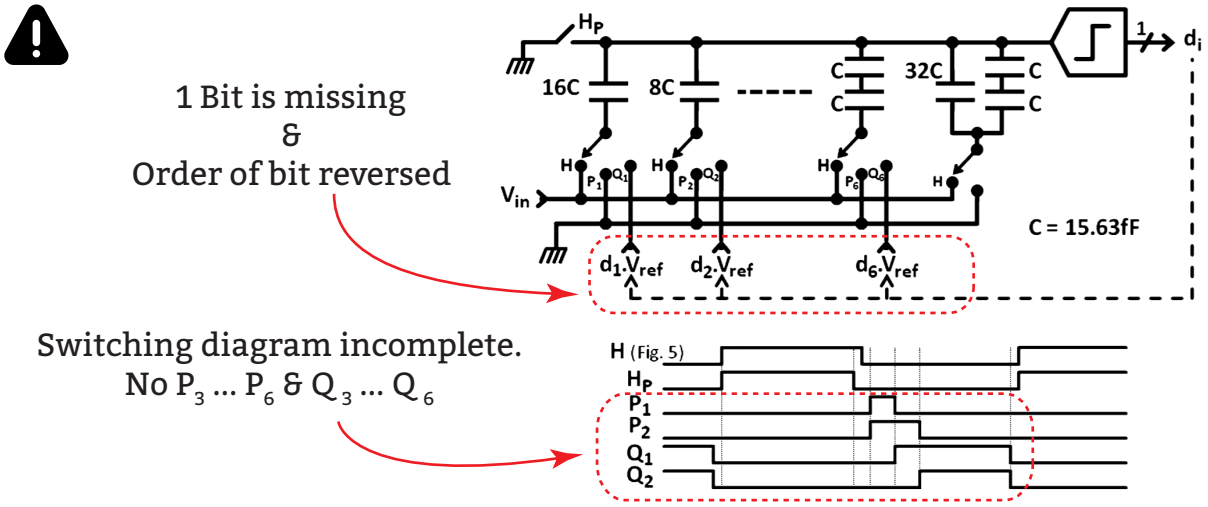


Fig. 6. Second-stage 7b SAR ADC with half-reference architecture.

Figure 11: Figure adapted from the reviewed article

2.2.1 Analysis of the Half Reference SAR

Since the principle of function is analogous to the SAR of the first stage, in this section is discussed how the changes made to the standard SAR structure allow the digital conversion without introducing the extra reference voltage. For this purpose we will consider the determination of the MSB. From the equivalent circuit of Figure 12 the following charge conservation equation may be deduced:

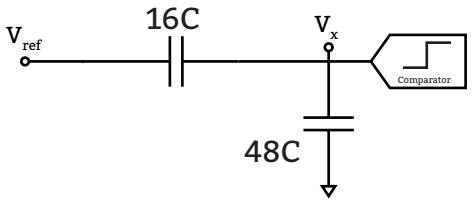


Figure 12: Second Stage: Equivalent circuit during the MSB Conversion

$$-64CV_{in} = (V_x - V_{ref})16C + V_x 48C$$
$$V_x = -V_{in} + \frac{V_{ref}}{4} \tag{6}$$

Equation 6 shows that the introduced modification avoids to introduce the extra reference voltage.

2.3 Digital Correction Block

Despite this block is not explicitly discussed in the article, a simple way to combine the bits from the two stages, is to perform the following operation in the digital domain:

$$D_{out} = D_1 + \frac{1}{2^{B_{1eff}}} D_2 \tag{7}$$

where D_1 and D_2 are the bits from stage one and two, respectively. B_{1eff} is the effective number of bits for the first stage.

3 Analog Building Blocks

3.1 The Amplifier

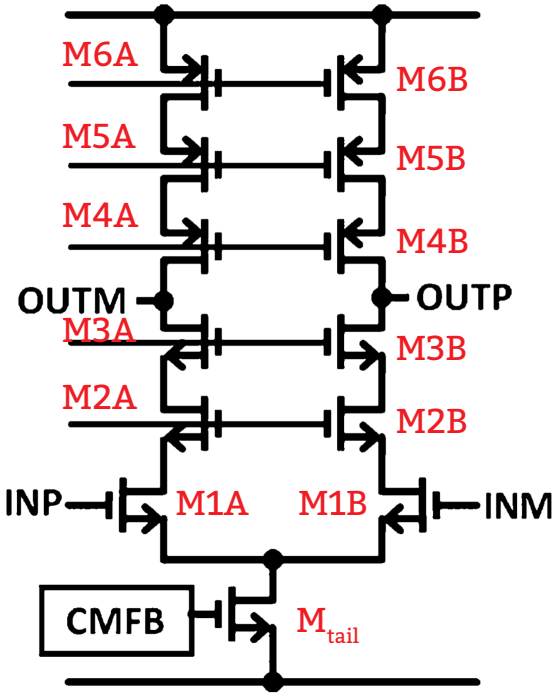


Figure 13: Amplifier

The amplifier used for the first stage is a fully differential telescopic cascode. The gate of the tail transistor is the common mode control terminal. At lower frequency the open loop gain A_{v0} of the amplifier is:

$$A_{v0} = g_m^{M1} R_{out} \tag{8}$$

where

$$R_{out} = r_o^{M1} \left(g_m^{M2} r_o^{M2}\right) \left(g_m^{M3} r_o^{M3}\right) || r_o^{M6} \left(g_m^{M4} r_o^{M4}\right) \left(g_m^{M5} r_o^{M5}\right)$$

The dominant pole of the system w_{dom} is (open loop):

$$\omega_{dom} = \frac{1}{C_L R_{out}} \tag{9}$$

where C_L denotes the capacitive load of the amplifier. We can approximate [2] the open loop transfer function as a first order system:

$$A_{OL}(s) = \frac{A_{v0}}{1 + \frac{s}{\omega_{dom}}} \tag{10}$$

The unity gain frequency ω_u of the amplifier can be approximated as[3]:

$$\omega_u \approx A_{v0}\omega_{dom} = \frac{g_m^{M1}}{C_L} \tag{11}$$

Equation (10) can be approximated at mid-band frequency as:

$$A_{OL}(s) \approx \frac{\omega_u}{s} \tag{12}$$

The closed loop response of the system is

$$A_{CL}(s) = \frac{A_{OL}(s)}{1 + \beta A_{OL}(s)} \approx \frac{\omega_u}{s + \beta\omega_u} \tag{13}$$

where β is the amount of feedback. The -3dB frequency of the system is thus:

$$\omega_{-3dB} = \beta\omega_u = \beta\frac{g_m^{M1}}{C_L} \tag{14}$$

The slew rate (SR) of the amplifier is

$$\mathrm{SR} = \frac{I_{tail}}{C_L} \tag{15}$$

For the topology under analysis, the following advantages may be recognized:

- Only NMOS transistor conduct time varying currents, this allows the amplifier speed to be maximized. Usually folded cascode counterpart, are two or three time slower.
- Telescopic amplifiers have limited output swing. The considered amplifier has an output swing of 390 $\mathrm{mV_{pk-pk}}$ and fits the 250 $\mathrm{mV_{pk-pk}}$ requirement. The footnote 9 at page 865 states:

[2] A more detailed analysis shows that the system has other non-dominant pole, for example the one created at the interface of M1A and M2A
[3] We assume $\omega_u \gg \omega_{dom}$

To accommodate comparator offsets allowed by redundancy, a larger swing would be required. For a worst case comparator offset an output swing of 500 mV is required.

There is an apparent inconsistency between the 500 mV requirement and 390 mV output single ended voltage swing of the amplifier. In general, higher swing requirement may be achieved by using a folded cascode architecture.

- If the voltage supply drops to 80%, the output swing lowers to 130mV and **no longer matches the given specification**.
- In general the designer, to match SNR specification, may compensate the limited signal swing by increasing capacitor size.
- The Author proposed a single stage amplifier and this usually reduces the power requirements.
- It may be proven that the telescopic cascode, with respect to other single stage topology, is the best choice with respect to noise contribution. Noise contribution of the circuit are due to M1 and M6. The input referred noise spectral density is:

$$S_{Vin}(f) = \frac{16}{3} kT \frac{1}{g_m^{M1}} \left(1 + \frac{g_m^{M6}}{g_m^{M1}}\right) \tag{16}$$

The input referred random noise offset is described as:

$$\sigma^2_{V_{in}} = \sigma^2_{VT1} + \frac{g_m^{M6}}{g_m^{M1}} \sigma^2_{VT6} \,. \tag{17}$$

Independently from architecture, a high gain OTA is a *power-hungry* block. To overcome this pitfall and thus to further reduce the power consumption, some researchers [4] have proposed to implement the gain stage by means of a cascade of capacitive charge pump cell. A capacitive charge pump cell is depicted in Figure 14:

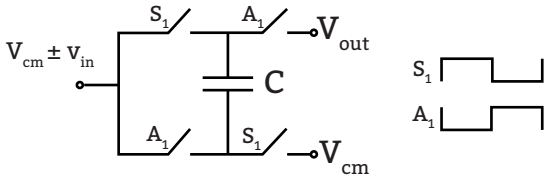


Figure 14: The charge pump cell

From the conservation of charge the following equation is deduced

$$\begin{aligned} (V_{out} - (V_{cm} \pm v_{in}))C &= \pm v_{in} C \\ V_{out} &= V_{cm} \pm 2v_{in} \end{aligned} \tag{18}$$

Equation 18 shows that the charge pump cell has a gain of 2. This means that we can cascade this cell to get higher gain as shown in Figure 15.

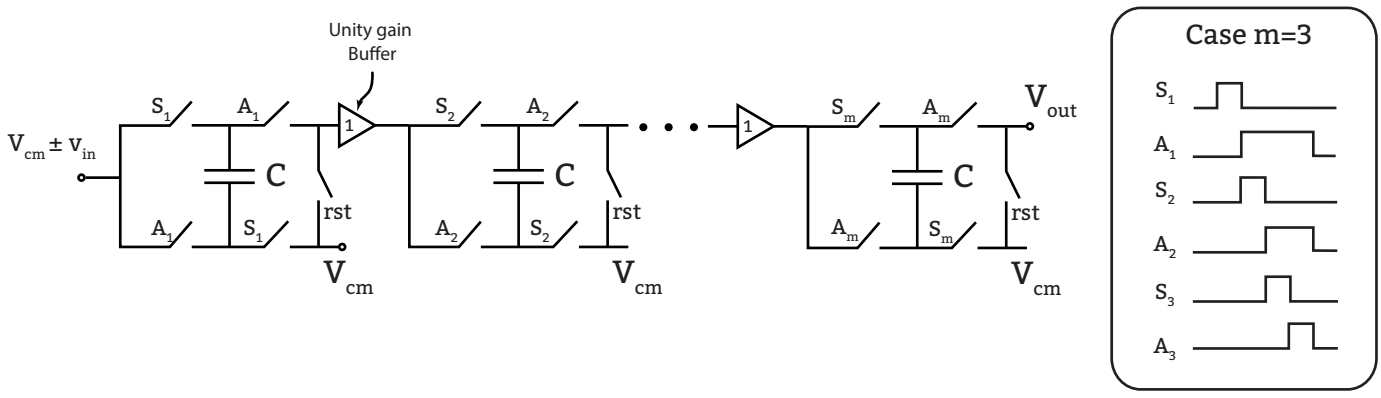
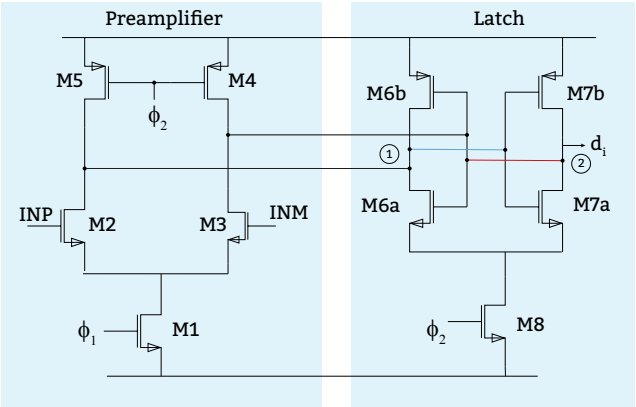


Figure 15: Cascade of charge pump cell. Figure adapted from [4].

3.2 The Comparator of Stage 1 SAR Sub-ADC

The comparator introduced by the Authors is *dynamic preamplifier* based. Its circuit is displayed in Figure 16. A standard dynamic latch has beeen exclude because, the stack of 4 transistor slows down the comparison process. In fact, a high input common mode gate voltage cannot be chosen to force a quick decision.



The comparator is composed of an amplifier followed by a latch. The amplifier is implemented by means of differential pair and the latch is a cross coupled CMOS inverter (positive feedback).

Figure 16: Dynamic preamplified-based comparator

Two phases of operation can be recognized:

- ϕ_1 HIGH and ϕ_2 low: the preamplifier is on (M2 and M3 in saturation, M4 and M5 in triode) and latch is deactivated. The input voltage is amplified onto the input nodes of the latch, with a common mode near V_{dd}.
- ϕ_1 low and ϕ_2 HIGH: the preamplifier is off and the latch is on. Thanks to the latch positive feedback, the voltage difference between node 1 and 2 will set the output of the latch either to $V_d d$ or GND.

Latch mode time constant

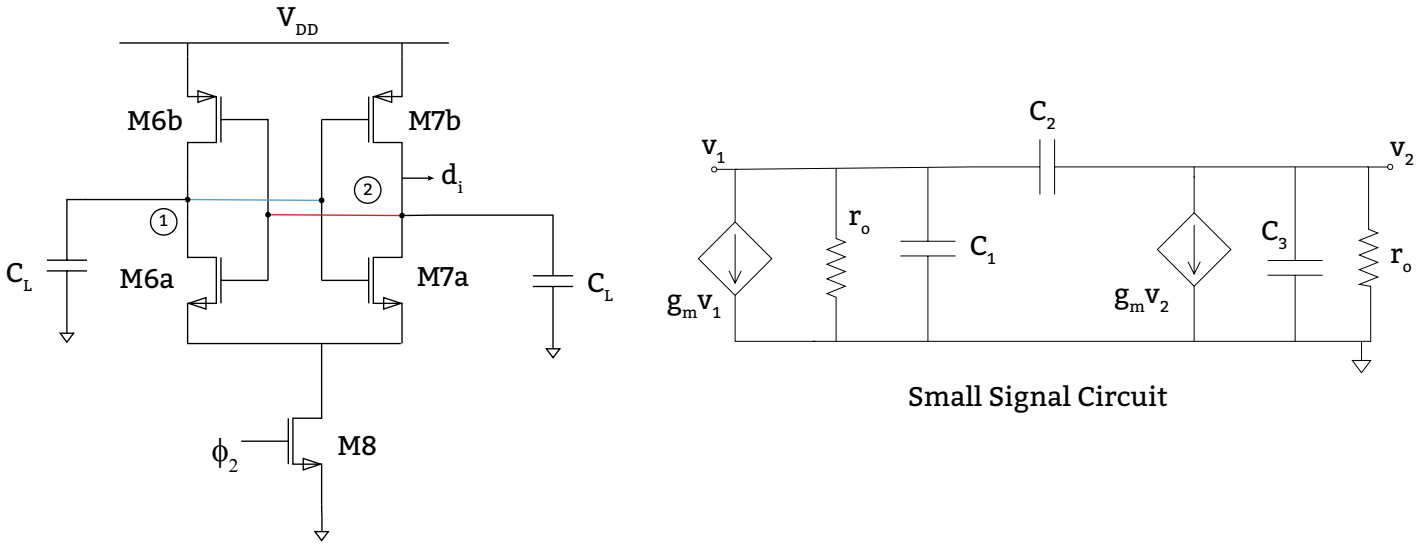


Figure 17: Comparator equivalent circuit during ϕ_2 phase

In the following we will derive an expression for the conversion time needed by the latch. At the end of the ϕ_1 phase the comparator can be considered as in Figure 17, where C_L is the capacitance of the previous stage. From the analysis of the small signal circuit of Figure 17 we deduce the KCL equation at node 1 and 2:

$$g_m v_1 + g_o v_1 + C_1 \frac{\mathrm{d}v_1}{\mathrm{d}t} + C_2 \frac{\mathrm{d}\,(v_1 - v_2)}{\mathrm{d}t} = 0 \tag{19a}$$

$$g_m v_2 + g_o v_2 + C_1 \frac{\mathrm{d}v_2}{\mathrm{d}t} = C_2 \frac{\mathrm{d}\,(v_1 - v_2)}{\mathrm{d}t} \tag{19b}$$

to simplify our analysis the following assumptions / positions are made:

$$g_m^{M6b} = g_m^{M7b} = g_{mp} \qquad C_{gs}^{M6b} = C_{gs}^{M7b} = C_{gsp} \qquad C_{gd}^{M6a} = C_{gd}^{M7a} = C_{gdn}$$
$$g_m^{M6a} = g_m^{M7a} = g_{mn} \qquad C_{gs}^{M6a} = C_{gs}^{M7a} = C_{gsn} \qquad r_o^{M6b} = r_o^{M7b} = r_{op}$$
$$g_m = g_{mn} + g_{mp} \qquad C_{gd}^{M6b} = C_{gd}^{M7b} = C_{gdp} \qquad r_o^{M6a} = r_o^{M7a} = r_{on}$$

$$\begin{aligned} C_1 &= C_L + C_{dbp} + C_{dbn} + C_{gsp} + C_{gsn} \\ C_2 &= 2\left(C_{gdp} + C_{gdn}\right) \\ r_o &= r_{op} || r_{on} = \frac{1}{g_o} \\ v_d &= v_1 - v_2 \end{aligned}$$

If equation 19b is subtracted from 19a:

$$\begin{aligned} \frac{\mathrm{d}(v_1 - v_2)}{\mathrm{d}t} &= \frac{g_m + g_o}{C_1 + 2C_2}\left(v_1 - v_2\right) \\ \frac{\mathrm{d}v_d}{\mathrm{d}t} &= \frac{g_m + g_o}{C_1 + 2C_2} v_d \end{aligned} \tag{20}$$

We assume that[4] $v_d(t=0) = v_{init}$ and the solution of Equation (20) is:

$$v_d(t) = v_{init} e^{\frac{t}{\tau}} \tag{21}$$

where τ :

$$\tau = \frac{2C_2 + C_1}{g_m} = \frac{C_L + C_{dbp} + C_{dbn} + C_{gsp} + C_{gsn} + 4(C_{gdp} + C_{gdn})}{g_{mp} + g_{mn}} \tag{22}$$

In order to reduce the comparator decision process τ needs to be minimized. Thus the length of latch transistors should be as small as possible. Unfortunately, the smaller the transistor length the higher the input referred offset voltage. Thus, a trade off between comparator accuracy and speed is necessary.

Kickback

Because the drains of M2 and M3 are directly connected to the regeneration nodes, the comparator of Figure 16, suffers from kickback noise. This means that nodes that are capacitively coupled to input have rail to rail variations. However, such direct connection makes the comparator reacts faster to variations. As observed in [5], *the fastest and more power efficient comparators generate more kickback noise*. From considerations done in [5], we can modify the proposed comparator to reduce the kickback noise as follows:

- by introducing switches that isolate the drain of M2 and M3 during the regeneration phase;
- by applying a neutralization techniques to the feedback capacitance of M2 and M3 (gate-drain capacitance).

The actual implementation of the previous changes is shown in Figure 18.

[4] with $t = 0$ we mean the time when the latch is activated

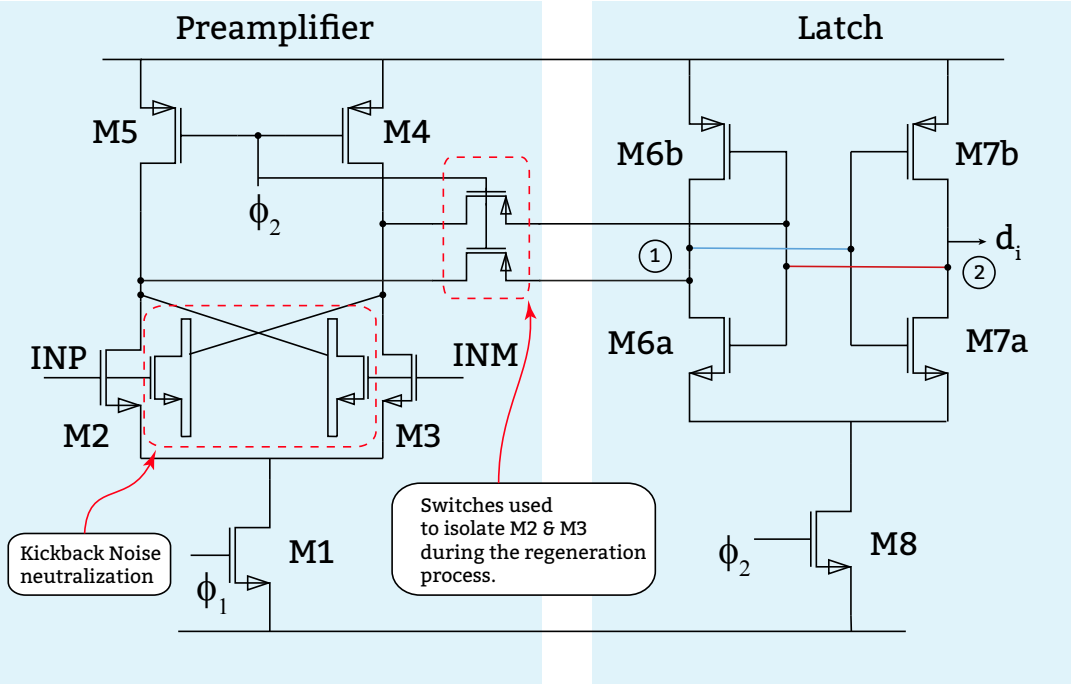


Figure 18: Modified comparator to reduce the kickback noise

4 Measurement & Results

The Authors provided the measurement of INL, DNL and the power spectra (see Figures 12 a 13 of the paper). Because of the predominance of odd-order harmonics, the S shape of the INL plot is consistent with the spectra. From the spectra we also observe that SFDR = 78dB. The DNL is less then 1 LSB, thus the converter is monotonic and there are no missing codes. The SINAD is provided for both 65nm and 90nm technology. The ENOBs of the converter, in 65nm and 90nm technology, respectively are:

$$ENOB_{65\text{nm}} = \frac{66 - 1.76}{6.02} = 10.7\text{b} \qquad ENOB_{90\text{nm}} = \frac{65.6 - 1.76}{6.02} = 10.6\text{b} \tag{23}$$

From the information provided in the article, the following figures of merit can be computed for the provided technologies:

$$\text{F.o.M}_{65\text{nm}} = \frac{P}{f_s 2^{ENOB}} = 52 \frac{\text{fJ}}{\text{conversion} - \text{step}} \qquad \text{F.o.M}_{90\text{nm}} = \frac{P}{f_s 2^{ENOB}} = 53 \frac{\text{fJ}}{\text{conversion} - \text{step}}$$

With reference to timeline .vs. F.o.M. reported by Pelgrom [1](p.119, Figure 4.19) the current architecture is judged as competitive. The measurements are enough to compute all the usual indices of merit for a converter. However, to have a broad view of performances, the Authors could have mentioned about the previous technology. Such a review dealing with pipeline ADC is available in reference [7]. We observe that only 19% of reviewed articles achieve 12 bits of resolution.

4.1 Synthetic review of 12 bit pipeline ADC

The Table 1 has been compiled with, info collected from different references. It allows a direct comparison of some data converter performance.

Reference	Peak INL (LSB)	Peak DNL (LSB)	Sampling Rate	SNDR(dB)	SFDR(dB)	Power Diss. mW	Technology	Area mm^2
[2]	1.50	1.20	110 MS/s	64.2	69.4	97	0.18u CMOS	0.86
[6]	0.24	0.09	80MS/s	72.6	84.5	755	0.25u CMOS	22.60
[8]	0.75	0.42	20Ms/s	70.2	80.3	231	0.35u CMOS	7.50
[9]	0.47	0.41	20Ms/s	70.8	93.3	226	0.35u CMOS	7.50
[3]	3.00	0.50	3Gs/s	58.0	-	500	40nm CMOS	0.40
Rev. Article	1.50	0.75	50Ms/s	65.5	78	3.5	65nm CMOS	0.16
Rev. Article	1.60	0.80	50Ms/s	65.6	77	3.6	90nm CMOS	0.16

Table 1: 12b Pipeline ADC Review

The proposed architecture has a competitive DNL and SNDR specifications. The power requirement is minimum with respect to other reviewed architectures. It is also worth to mention that the referenced papers, report about structures achieving the reported INL and DNL specifications by means of calibration. On the other end the proposed structure is **calibration free**.

4.2 Technology dependence

Notwithstanding the measurements show little dependence on transistor technology, the Authors report that the topology for 65nm is slightly different from 90nm. In fact, in 65nm technology, the half reference architecture is not introduced. The Authors do not discuss in detail the effects of the f_t and the mismatch of the transistor. However, due to presence of positive feedback, transistors of the latch and differential pair of the comparator in Figure 16, should be implemented with the lowest possible mismatch in the threshold voltage.

5 Curiosity

The industrial interest of the proposed architecture is witnessed by US patent `US20130321184A1`, filed in 2012. The article and its Authors are never mentioned in the patent.

References

[1] Marcel J.M. Pelgrom (auth.) *Analog-to-Digital Conversion*. 3rd Edition. Springer Netherlands, 2016.

[2] Terje N. Andersen et al. "A 97mW 110MS/s 12b pipeline ADC implemented in 0.18μm digital CMOS". In: *Proceedings -Design, Automation and Test in Europe, DATE '05* 2005.Cm (2005), pp. 219–222. ISSN: 15301591. DOI: 10.1109/DATE.2005.3.

[3] Chun Ying Chen et al. "A 12-Bit 3 GS/s pipeline ADC with 0.4 mm 2 and 500 mW in 40 nm digital CMOS". In: *IEEE Journal of Solid-State Circuits* 47.4 (2012), pp. 1013–1021. ISSN: 00189200. DOI: 10.1109/JSSC.2012.2185192.

[4] Kairang Chen and Atila Alvandpour. "Design of a gain-stage for pipelined SAR ADC using capacitive charge pump". In: *Proceedings of the 23rd International Conference Mixed Design of Integrated Circuits and Systems, MIXDES 2016* 2 (2016), pp. 187–190. DOI: 10.1109/MIXDES.2016.7529729.

[5] Pedro Figueiredo and João Vital. "Kickback noise reduction techniques for CMOS latched comparators". In: *Circuits and Systems II: Express Briefs, IEEE Transactions on* 53 (Aug. 2006), pp. 541–545. DOI: 10.1109/TCSII.2006.875308.

[6] Carl R. Grace, Paul J. Hurst, and Stephen H. Lewis. "A 12b 80MS/s pipelined ADC with bootstrapped digital calibration". In: *Digest of Technical Papers - IEEE International Solid-State Circuits Conference* 47 (2004). ISSN: 01936530. DOI: 10.1109/isscc.2004.1332793.

[7] Tanvir Hussain, Md Ghulam Zakir, and Md Rafiqul Islam Sheikh. "State-of-the-art pipeline A/D converter survey and analysis". In: *2012 International Conference on Informatics, Electronics and Vision, ICIEV 2012* (2012), pp. 476–481. DOI: 10.1109/ICIEV.2012.6317457.

[8] Haoyue Wang et al. "Nested digital background calibration of a 12-bit pipelined ADC without an input SHA". In: *IEEE Journal of Solid-State Circuits* 44.10 (2009), pp. 2780–2789. ISSN: 00189200. DOI: 10.1109/JSSC.2009.2028756.

[9] Xiaoyue Wang, Paul J Hurst, and Stephen H Lewis. "A 12-Bit 20-Msample / s Pipelined Analog-to-Digital Background Calibration". In: *IEEE Journal of Solid-State Circuits* 39.11 (2004), pp. 1799–1808.

[10] Wenhua Yang et al. "A 3-V 340-mW 14-b 75-Msample/s CMOS ADC with 85-dB SFDR at Nyquist input". In: *IEEE Journal of Solid-State Circuits* 36.12 (2001), pp. 1931–1936. ISSN: 00189200. DOI: 10.1109/4.972143.