Assignment 3 - Pietro Pennestrì s2382660

TES 1

The simulation of Figure 1 depicts the propagation of an `x` into the scan chain. The `x` is propagated from `scan_in` port to `scan_out` as in a FIFO memory. In the considered simulation, the `scan_shift` signal is always high. Thus outputs from the combinatorial circuit are ignored.

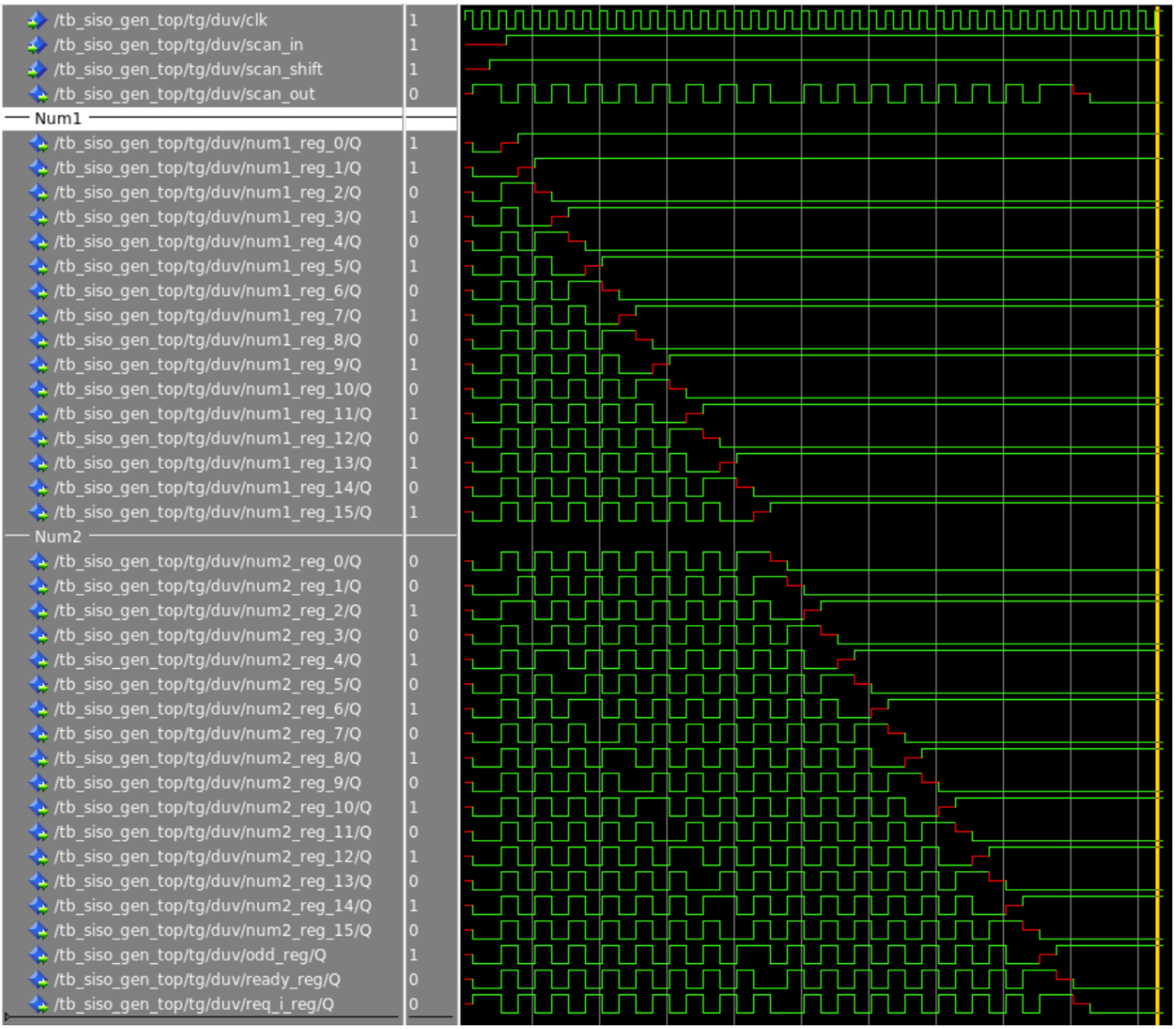

Figure 1: `gcd` architecture with a scan in - scan out architecture

TES 2

The `swap` architecture has the following behaviour:

The output data for an input sequence

$$i = d_0, d_1, \cdots, d_n, n \geq 1$$

will generate an output sequence

$$o = 0, 0, d1, d0, d3, d2, \cdots, d_{2k+1}, d_{2k}, d_{2k+1}, d_{2k+3}, d_{4k}, \cdots \quad (1)$$

The request data signal `req` is always raised high. The `ready` signal is low only during the reset phase and in the first clock cycle after `reset` is raised low.

State	Code : `State[1] State[0]`
start	00
odd	01
even	10

The block diagram corresponding to the `swap` architecture is depicted in Figure 2.

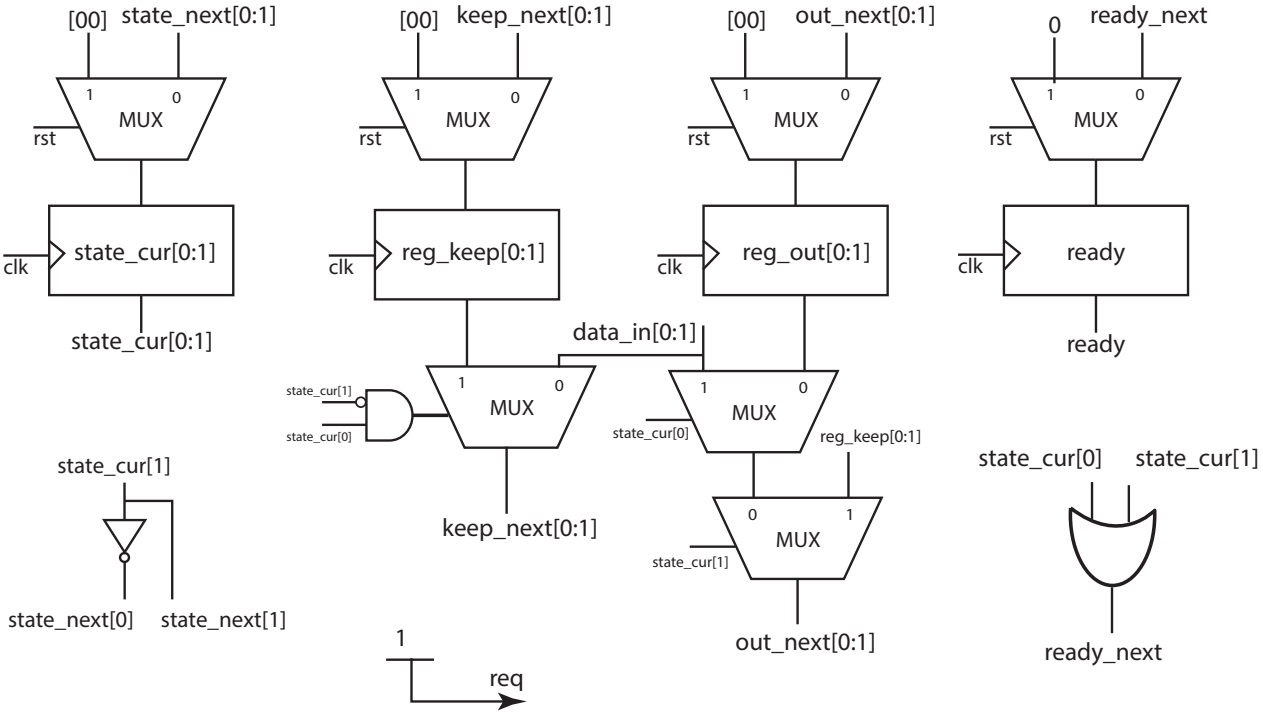

Figure 2: Block diagram of `swap`

TES 3

The node under investigation is `n3` and a *stuck at 0* fault is considered. The annotated version of the `swap` circuit is depicted in Figure 3.

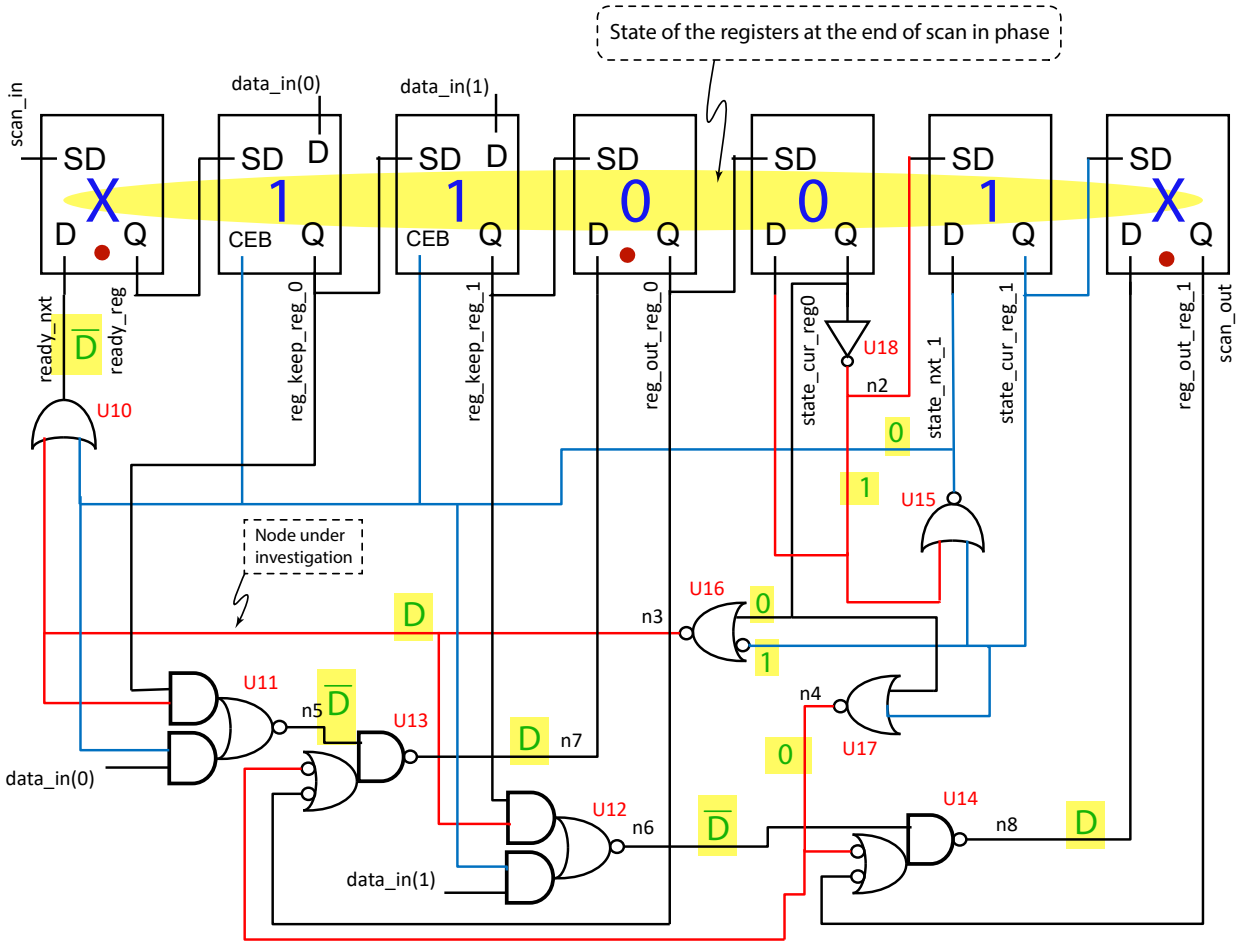

Figure 3: `swap` circuit

As indicated in Figure 3, the input of the combinatorial circuit is x11001x (`ready_reg ... reg_out_reg_1`). The pattern provided to `scan_in`, to obtain this state at the end of the scan in phase, is:

x (first element), 0, 0, 0, 1, 1, x (last element).

If a *stuck at 0* fault is preset in `n3` then, during the *capture* phase, the content of `ready_reg`, `reg_out_reg_0` and `reg_out_reg_1` is wrong. Despite not affected by error, the content of other registers can be read at the `scan_out` port during successive clock cycles. This test pattern can also be used to determine a *stuck at 1* in `state_nxt_1` node. The `swap` circuit has in his scan in - scan out chain two successive flip flops with an enable signal. However, if those two flip flops are not enabled, it is still possible to detect an error. In particular, the value of `ready_reg`, which precedes the enabled signals flip flop, can be accessed from the output ports.

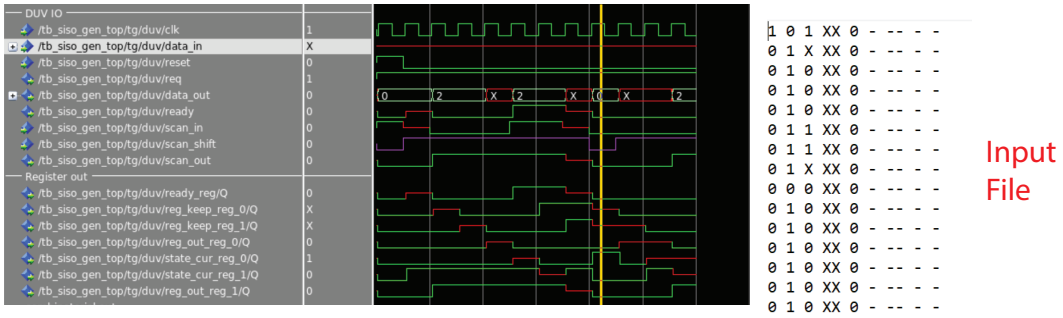

Figure 4: Scan in - Scan out operation when no faults are present in the circuit

The table below summarizes the result of a scan in - scan out operation when no error is introduced in the system. The simulation waveform is depicted in Figure 4.

ready	keep0	keep1	out0	state0	state1	out1=scan_out	
x	1	1	0	0	1	x	← State of the registers at the end of scan in operation
1	x	x	1	1	0	1	← State of the registers during capture phase
0	1	x	x	1	0	0	← State of the registers at the beginning
0	0	1	x	x	0	0	of shift out phase
0	0	0	1	x	x	0	
0	0	0	0	1	x	x	
0	0	0	0	0	0	x	
0	0	0	0	0	1	0	← State of the registers at the end of shift out phase

Table 1: Expected value for a test pattern x11001x and no faults present in the circuit

The simulation result when the fault is introduced in `n3` is depicted in Figure 5.

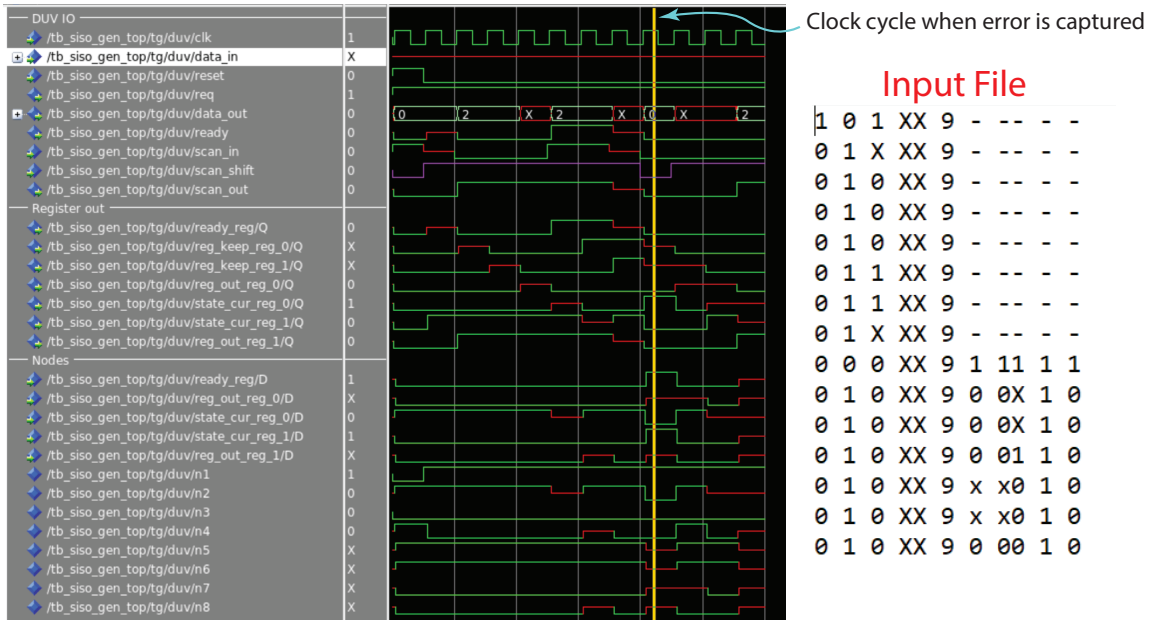

Figure 5: Scan in - Scan out operation when a fault in `n3` is present in the circuit

During the capture operation some of the faults introduced in the system are detected. In particular, `data_out` and `ready` port have fault values. The (correct) expected value of `data_out= "11"`, but `"00"` is read. For `ready ='1'` expected, `ready ='0'` is read.

```
VSIM 23> do wave.do
VSIM 24> run -all
# ** Note: Output error for signal scan_out at line nr. 9; expected: 1; read: 0
#    Time: 44900 ps  Iteration: 0  Instance: /tb_siso_gen_top/tg/tvc
# ** Note: Output error for signal data_out at line nr. 9; expected: 11; read: 00
#    Time: 44900 ps  Iteration: 0  Instance: /tb_siso_gen_top/tg/tvc
# ** Note: Output error for signal ready at line nr. 9; expected: 1; read: 0
#    Time: 44900 ps  Iteration: 0  Instance: /tb_siso_gen_top/tg/tvc
# ** Note: Output error for signal data_out at line nr. 10; expected: 0X; read: 0X
#    Time: 49900 ps  Iteration: 0  Instance: /tb_siso_gen_top/tg/tvc
# ** Note: Output error for signal data_out at line nr. 11; expected: 0X; read: 0X
#    Time: 54900 ps  Iteration: 0  Instance: /tb_siso_gen_top/tg/tvc
# ** Note: Output error for signal scan_out at line nr. 12; expected: 0; read: 1
#    Time: 59900 ps  Iteration: 0  Instance: /tb_siso_gen_top/tg/tvc
# ** Note: Output error for signal data_out at line nr. 12; expected: 01; read: 10
#    Time: 59900 ps  Iteration: 0  Instance: /tb_siso_gen_top/tg/tvc
# ** Failure: Input error while reading signal scan_out at line nr. 13
#    Time: 60 ns  Iteration: 0  Process: /tb_siso_gen_top/tg/tvc/stimuli File: /home/s2382660/tes/tvc_siso_gen_tester_arch.vhd
# Break in Subprogram check_read at /home/s2382660/tes/tvc_siso_gen_tester_arch.vhd line 64
```

Figure 6: `Modelsim` log generated during the simulation